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EXAMINER	
PADGETT, MARIANNE L	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,648	CHOE ET AL.	
	Examiner	Art Unit	
	MARIANNE L. PADGETT	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,8-11,16-24,27-30,34,39 and 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-6,8-11,16-24,27-30,34,39 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/4/8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. A **Request for Continued Examination** under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on **6/4/2008** has been entered.

The examiner notes that claim 39 is formally noncompliant, as the previous version of claim 39 ended with the phrase "from the dopant region", which is no longer in the claim, but has not been formally deleted by strike-through, however as what has been added to the claim was underlying, is consistent with the language of new independent claim 40, replaces the missing words with an equivalent meaning & make sense as written, it appears to the examiner to have been consistent with applicant's intent & the claims will be considered by the examiner without sending out a noncompliant letter.

The amendment, as noted in the advisory of 6/2/2008 appears to correct problems set forth in previous 112 first & second rejections of sections 2-4 of the action mailed 3/14/2008, but creates potential new problems as detailed below. It also overcomes all prior art as set forth in previous rejections, except Hodge et al., which requires further considerations as discussed below. Generally, it is noted by the examiner that the Ikeda, Hiromitsu & Houston references do not provide teachings concerning the second ion implanting; and Bendernagel et al. & Sadana, while contemplating multiple ion implantings, do not perform them with the right combinations of types ions for the claims as now written.

The amended claims appear to include new matter, & as was noted that for the claims as written, where the first ion implanting with dopant & the second ion implanting with Si or Ge or Ne or Bi or Sn or Xe can be done at different times with respect to the annealing, which is only necessary to activate the p- or n-type dopant implants, such that when the second ion implantation is performed, is not limited. The process of Hodge et al. (5,387,541), which anodizes a doped silicon substrate (may have been implanted & annealed to activate) to create a porous layer, which may be then implanted with claimed second

implanting ions (Si or Ge) & then oxidized at temperatures overlapping with those claimed, hence it appears that Hodge et al. is still applicable under 103 considerations, as discussed below. One new issue that needs to be discussed with respect to Hodge et al., in the anodization limitation is the issue of the depth (>50 nm) at which porosity of claim percentage ranges are produced, which is supported in the cited [0047-53], especially [0051 & 53].

2. **Claims 4-6, 8-11, 16-24, 27-30, 34 & 39-40** are rejected under 35 U.S.C. **112, first** paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 4-6, 8-11, 16-24, 27-30, 34 & 39-40 rejected under 35 U.S.C. **112, second** paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The typographical error of "Hf" instead of a --HF-- in new claim 40 with respect to the anodization limitation, is technically New Matter as written, since "Hf" stands for the element hafnium, thus makes literal sense as written, but is not supported by the original specification, nor is it scientifically supported that a hafnium solution is used for anodization. For purposes of examination over prior art, the "Hf" will be treated as -- HF --, as is consistent with the specification & indicated was intended by applicant during the interview of 5/21/2008.

In lines 2-3 of new claim 40, the dopant ion implantation "to a depth ranging from about 250 nm to about 1500 nm from a top of the Si-containing substrate" is only partially supported, as it is noted that the support in [0039], which references fig.1A, ref.# 12, appears to be indicating that these values represent approximately the depth at which the **implanted region starts and stops**, i.e. the bounds of its thickness, however the claims as written could indicate this, or could be indicating that this is a range

representing possible maximum depth to which the first implantation occurs, i.e. about 0-250 nm, up to about 0-1500 nm, which are very different meanings, such that this claim limitation is ambiguous & due to its ambiguity encompasses subject matter that is not clearly supported by the original specification, i.e. encompasses New Matter.

Claim 40's limitation concerning the "second ion implanting" (lines 4-5), which is discussed in paragraphs [0040-41] of the specification & original claims 31-32 contains the New Issue of the location of these ions with respect to the implanted dopant ions, where it is also noted that while the sequence of the steps as recited could imply an order in which individual limitations are intended to be performed, when the second ion implanting occurs is not actually **necessitated** in the claims, however in the cited support of the specification, [0042] clearly indicates via its temporal language "**Next**, the structure... is annealed..." (emphasis added), that the two ion implanting steps occur before the annealing, which is not necessitated by the language of claim 40, hence produces the additional issue of New Matter for the process as now presented in claim 40, as the overall process, which is basically consistent with the disclosed sequence of steps in the specification, is not supported for the **breath** of possible times at which the second ion implantation limitation may be performed with respect to all other steps in the process as presently claimed. Note, while the original claims separately contained two different ion implanting steps, which due to their lack of any association had no timing with respect to each other, these original claims cannot be considered to provide clear support for the context of presently amended claims.

In the thermal oxidizing limitation, on lines 15-17 of claim 40, which is discussed in the cited [0058-62] paragraphs of the specification, the examiner notes that [0058] specifically discloses that not all of the porous layer is converted into buried oxide layer, but that only the finer porous region becomes buried oxide 20, while the coarser porous silicon region typically coalesces into monocrystalline silicon, becoming part of the overlying silicon-containing overlayer 22 (figures 1C-1E). Since the graded porosity structure with finer & coarser porosity is taught in the preceding paragraphs to come from the

use of the dual ion implanting procedure, which is incorporated into claim 40, the claim of converting all of the porous region into a buried oxide region raises would appear to be **New Matter**, as it would appear to require forming a thicker buried oxide layer than appears to be contemplated or supported by the sequence of steps which applicant has cited as support in the original specification.

Also, as discussed in the interview of 5/21/2008, the claims 4-6 dependent claim sequence, raises the issue of whether or not the p-type dopant is intended to be positively claimed or remain optional in these dependent claims. At present, the explicit presentation of claims only directed to the specific p-type dopants in claims 4-6 provides the appearance of an intent to positively claim these limitations, however the language of these claims in lacking positive requirement of choice of the p-type dopant option, making the record un backspace clear.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. **Claims 4-6, 8-11, 16-24, 27-30, 34 & 39-40** are rejected under 35 U.S.C. 103(a) as obvious over **Hodge et al.** (5,387,541), in view of **Hiromitsu et al.** (JP 62-245620, English translation) & optionally considering Bendernagel et al. (6,800,518 B2).

Hodge et al. teach various possible routes for creating a porous layer within the silicon substrate, which may be oxidized so as to form a buried silicon layer. It is noted that in col. 1, lines 35-40, comments concerning the expense & difficulty to control porosity for layers of thickness of less than 0.25 μm (i.e. 250 nm), which value limit & subject would appear to be relevant to the ambiguity noted for the depth of the dopant ion implantation in new claim 40, since the dopant depth is intricately related to the subsequently created across the location & thickness. Specifically in Hodge et al., see the abstract; figures, noting figure 1 is a flow diagram suggesting various process routes, figure 2 illustrates blanket treatment, while figures 3 & 4 illustrate pattern treatments. Col. 1 discusses known prior art porosity treatments, teaching that dopant level determines number & size of pores (col. 1, lines 8-17), with discussion of porosity levels, such as less than 50% (col. 1, lines 37). The paragraph bridging cols. 1-2 discusses the importance of eliminating nonuniformity, while col. 2, lines 14-31 sets forth the basic process sequence of manufacturing a porous silicon layer in the silicon wafer, then ion implanting into the porous layer causing amorphization therein, followed by recrystallization/annealing, which may provide silicon-on-porous silicon material, that may be considered consistent with the dependent claims 16-17

step of forming a Si-containing cap layer on the substrate after the anodization process. Col. 2, lines 36-68 & col. 5, lines 30-48 discussed electrolytic anodization using hydrofluoric acid (HF), with an exemplary current density of 5.5 mA/cm^2, resulting in porous density of 1.17 g/cm^3 to a depth of 2.6 μm (i.e. >50 nm), with col. 3, lines 1-3 teaching "pre-anodization p+ implant of the non-porous silicon surface and annealed in order to enhance uniformity of current flow through the wafer during anodization", which is considered to read on ion implanting a dopant (≡ first ion implantation), activation thereof by annealing. Plus it was noted that ion implantation will inherently creating a gradient effect in the porosity since ion doping will create a gradient concentration of dopant over a range of implantation depths.

In col. 3, lines 4-53 & col.5, lines 49-col. 6, lines 3, after annealing & anodization Hodge et al. teaches ion implantation (≡ second ion implantation) that may include ions, such as **Ge$^+$**, **Si$^+$**, Sn$^+$, etc., where typical doses are taught to be **>10^{14} ion/cm^2**, used to produce an amorphous layer which may be part of or the entire depth of the porous silicon layer & multiple ion implantations may be employed. While a particular range of ion energies is not taught, an exemplary ion implantation condition of 10^{16} Ge$^+$/cm^2 at 80 keV followed by 10^{16} F$^+$/cm^2 at 35 KeV was given, hence while the example is not of an energy in dependent claim 34's range, the particular example would not have been considered limiting by one of ordinary skill of the art, since in order to perform the taught range of various implantation depths that include partial to complete overlap of depth with the porous silicon, one of ordinary skill would reasonably have been expected to adjust their ion energy according to the particular ion & specific depth to which they wish to implant, thus useful Si or Ge ion implantation energies would have been expected to encompass claimed second ion implantation energies, dependent on desired depth & have been determined via routine experimentation. On lines 44-54, note optional use of masking to create amorphous silicon islands on porous silicon surface due to patterned implantation of the equivalent of the second ion implantation.

In col. 3, lines 58-64 & col. 6, lines 4-17 of Hodge et al., see discussion of typical annealing procedures, including preferred alternatives of 3 minutes rapid thermal annealing at 950°C in Ar and also 24 hours at 525°C in nitrogen or argon; col. 3, lines 65-col. 4, line 53 & col. 6, lines 56-col. 7, line 20 for various oxidizing procedures that may be employed when buried oxide layer, i.e. SOI material, is desired to be produced, including possible patterning (col. 4, lines 10-19), a stabilizing oxidation process annealing at 300°C for an hour in flowing oxygen (col. 4, lines 20-31), then a wet oxidation process that uses various sequences or temperatures, including wet oxidation at 800°C for two hours, followed by 1090°C wet oxidation four minutes, where wet oxidations may typically **include gases of H_2 & O_2** (col. 4, lines 32-54), thus encompasses oxygen & hydrogen ambient atmospheres. Applicant's various thermal oxidation & post oxidation steps appear overlap &/or encompass the various possible oxidation steps & sequences as taught by Hodge et al.

Hodge et al. does not explicitly state that the buried oxide layer, which they may produce, is "uniform" nor provide a degree of uniform as in applicants' specification definition, however as basically the same process steps as claimed are employ, the resultant effect would have been expected to be of analogous uniformity, whether one considers that term as a relative term, or within the scope of applicants' 20% thickness uniformity, as combined with defined upper & lower layers, which are consistent with the results of Hodge et al., especially considering their teachings on enhancing uniformity of current flow during anodization, which would have been expected to enhance uniformity of porous layer formation, thus uniformity of resultant buried layer formed therefrom. Alternately, it would've been obvious to one of ordinary skill the art to employ the taught process for making SOI structures so as to make sufficiently uniform, reproducible layers useful for semiconductor device formation. Also see above analogous discussions.

Hodge et al. differs from the new independent claim 40 by not designating a specific depth to which the n-type or p-type dopants used for the anodization/porosity techniques may be implanted, and

from dependent claims 4-6 in that while they generically note that in preparation for the anodization process for creating the porosity, p-type dopants may be implanted & annealed, they do not provide any further details of this step, suggesting that one of ordinary skill in the art would have been expected to be conversant with such procedures, such that it would have been obvious for one of ordinary skill in the art to employ techniques known in the art therefore.

The Japanese references to Hiromitsu et al. teach p-type ion implantation into silicon as preparation for creating porous silicon via electrolytic anodization, thus providing details concerning the ion implantation dopant process that one of ordinary skill the art would have expected to be relevant to Hodge et al. Hiromitsu's English abstract is generic with respect to the p-type dopant, but specifically illustrates annealing the ion implanted doped silicon before performing the anodic process in hydrofluoric acid. The translation of Hiromitsu et al. on pages 6-7 indicates B^+ ion implantation (ref. #7) & proton ion implantation (ref. #9, i.e. H+), then annealing at 400°C to form an n-type layer under the nitride pattern (ref #5), where porous silicon (ref #11) is formed by anodization in HF, such that areas with greater density (ref #10) are over areas of lower density in a pattern manner. Hiromitsu et al. discusses neither specific depths of implantation, nor specific thicknesses of implanted regions, or ion energies employed which would be intimately related thereto, however Hiromitsu et al. provides evidence of the known and expected usefulness of B^+ ion implantation for creating the require doped regions for electrolytic anodic creation of porous silicon for use in SOI structure formation as required in the process of Hodge et al., as well as the shown desirability of various configurations relating to density & porosity, hence illustrating the above discussed obviousness for dopants, such as B^+. As previously discussed, dependent claims differ by requiring specific dopants, such as B, instead of generic teachings of the patent & specific parameters for the implantation, however these would have been obvious variations relevant to routine experimentation & optimization of the process as taught by Hodge et al., in light of prior art suggestions such as those of Hiromitsu et al. and would not be considered to provide patentable significance to the

process, as such routine experimentation considerations of the teachings of Hodge et al. would have been expected to encompass such parameters given their teachings that produce analogous results from otherwise like steps.

More specifically with respect to the specifically claimed depth of implantation, or ambiguously bounds of the implantation region & parameters used therefore, while not specifically taught by Hodge et al. (& Hiromitsu et al.), one of ordinary skill in the art would have expected the depth to of been dependent on the particular device requirements, as the anodization technique's creation of porosity is dependent on the present & concentration of dopant, hence depth &/or thickness would have been dependent on where the particular device needed the SOI layer, with optimization of energies & doses following therefrom & determined to be a routine experimentation.

Alternatively, Bendernagel et al. (discussed in previous actions, see sections 10-11 of the action mailed 3/14/2008), who analogously provides SOI structures, supports the above assertions (column 5, lines 28-50 & column 6, lines 28-35) discussing preferred SOI thicknesses of 5 nm-1 μm (referred 5-200 nm) & porous layer thicknesses from anodized doped structures of about 100 nm-2 μm, hence it would've been further obvious to one of ordinary skill in the art to employ such teachings with the process of Hodge et al., including as combined with Hiromitsu et al. for particular dopants, in order to provide guidance on dopant implantation distribution during routine experimentation, while taking into consideration Hodges use of a second ion implanted species to modify the porous layer thickness due to amorphization of the porous layer structure, which thus modifies the resultant SOI layer is thickness, such that claimed depths, dopant ion energies & doses would have reasonably been expected to be employed in the taught process of the combination dependent on particular device considerations, especially considering suggested desirable porosity & SOI thicknesses Bendernagel et al. would have reasonably been expected to encompass claimed implantation depths. Furthermore, with respect to p-type ion dopant parameters Bendernagel et al. provide guidance of expected effective B concentrations (e.g. dose) for

analogous processing, teaching typical values of about 10^{15}-10^{19}, thus providing an obvious basis for routine experimentation for effective values dependent on particular device requirements.

5. The PGPub to Lin (2005/0045984 A1) cited by applicants, is noted to have relevant B ion implantation/anodization/oxidation teachings (abstract; [0014] & [0026]), specifically noting that boron ion doses of 10^{15}-10^{19} atoms/cm^2, creating p-type layers having a thickness of 4000-6000 Angstroms (i.e. 400-600 nm) after implantation & rapid thermal anneal, may be considered to provide cumulative or equivalent teachings & motivations as those provided by Bendernagel et al., with respect to the above rejection.

Zorinsky et al. (4,628,591) is the US version of JP 61-180446 cited by applicants, & is noted to teach the basic process for creating SOI structures via ion implantation using the n-type dopant phosphorus, with subsequent hydrogen fluoride anodization, then oxidation, including use of masking in order to create islands, but does not provide any teachings of specific parameters to employ, expecting one of ordinary skill in the art to be capable of parameter determination.

The English abstracts of Kaneko Shinichiro et al. (JP 62-108539 A) & Mizushina Yoshikiko et al. (JP 56-110247 A), which were cited by applicants in their 6/4/2008 PTO-1449 appear to be too processes that might be a relevant interest, however there is insufficient detail in the abstracts to determine if they are only of general interest or more, hence translations have been ordered.

6. Applicant's arguments filed 6/4/2008 & discussed above have been fully considered but they are not persuasive.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marianne L. Padgett whose telephone number is (571) 272-1425. The examiner can normally be reached on M-F from about 8:30 a.m. to 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Marianne L. Padgett/
Primary Examiner, Art Unit 1792

MLP/dictation software

6/18-19/2008